IN THE CLAIMS

Please amend the claims as follows:

1. (Original) An apparatus for processing data-items each associated with a respective data address in a range of data addresses, wherein compressed blocks representing the data items are stored in a memory system, memory addresses occupied by each block starting from a respective preferred starting address for multi address transfer of the memory system, each block representing compressed data-items associated with data addresses in a respective sub-range of the range, the sub-ranges being successively contiguous, each particular sub-range having a length corresponding to an address distance between the preferred starting address from which addresses of the particular block that represents the data-items in the particular sub-range start and the preferred starting address from which addresses of a next one of the blocks for a next successive sub-range start, leaving memory addresses not occupied by the particular block in between blocks, the apparatus comprising

- the memory system, which is capable of performing selectable length multi-address memory transfers starting from the preferred starting addresses only, or with less overhead than starting from other addresses than the preferred starting addresses;
- a processing element for processing the data-items;
- a decompressor coupled between the processing element and the memory system, the decompressor being arranged to
- start a multi address memory transfer of a required one of the blocks from the memory system dynamically when the processing element requires access to the block, leaving memory

addresses directly following the block up to a preferred starting address for a next one of the blocks untransferred in the transfer, and to

- decompress the data-items from the required one of the blocks before passing the data-items to the processing element.

2. (Original) An apparatus according to Claim 1, wherein the processing element is arranged to indicate, to the decompressor, a decompression option selected from a series of different decompression options that require successively less addresses starting from the preferred starting address of the required one of the blocks to be transferred, the decompressor setting the length of the memory transfer dependent indicated decompression option.

3. (Original) An apparatus according to Claim 1, wherein the decompressor is arranged to send a signal to the memory system to terminate the multi-address memory transfer of the required one of the blocks when a number of words, selected dependent on the length of the required one of the blocks, has been transferred.

4. (Original) An apparatus according to Claim 3, wherein the decompressor is arranged to retrieve information representing the length of the required one of the blocks from the multi address memory transfer, the decompressor generating the signal dependent on said information.

5. (Original) An apparatus according to Claim 1, wherein the decompressor is arranged to

- retrieve information representing the length of the required one of the blocks from a multi address memory transfer of

a precedingly retrieved block, retrieved preceding the required one of the blocks and to

- send a transfer length selection signal to the memory system derived from the information at the start of the multi address memory transfer for the required one of the blocks.

6. (Original) An apparatus according to Claim 1, wherein the lengths of the sub-ranges are mutually equal and larger than a distance between successive preferred starting addresses, the decompressor being arranged to start subsequent multi-address memory transfers for the required one of the blocks conditionally dependent on the length of the block.

7. (Original) An apparatus according to Claim 6, wherein each block comprises a plurality of sub-blocks that are decompressible independently of one another, each sub-block corresponding to a respective equal sized part of the sub-range for the block, the decompressor comprising a buffer memory region, for buffering the sub-blocks of compressed data read during the multi-address memory transfer, an intermediate memory region for storing data decompressed from the sub-blocks successively, the decompressor replacing the decompressed data from respective sub-blocks read during the memory transfer with one another successively in the intermediate memory.

8. (Original) An apparatus according to Claim 1, wherein the decompressor is arranged to apply decompression corresponding to lossy block compression.

9. (Original) An apparatus according to Claim 1, wherein the decompressor is arranged to apply decompression corresponding to variable length block compression.

10. (Original) An apparatus according to Claim 1, wherein the sub-ranges have mutually equal lengths.

11. (Original) An apparatus according to Claim 1, comprising a compressor for compressing the data items associated with respective ones of the sub-ranges that has a length equal to the distance between a pair of preferred starting addresses, the compressor compressing the data items associated with a respective one of the sub-ranges each into a respective one of the blocks, the compressor being arranged to store the compressed blocks into the memory system using a respective multi-address memory transfer for each respective one of the blocks, each transfer starting from a respective one of the preferred starting addresses, the decompressor terminating the multi-address memory transfers upon completion of storing each block, without writing up to a next preferred starting address when not required for the block.

12. (Original) An apparatus according to Claim 11, wherein the processing element computes the data-items for compression and the compressor is arranged to receive the data items for compression from the processing element.

13. (Original) An apparatus according to Claim 11, wherein the compressor is arranged to adapt a compression ratio for compression of the data dependent on a dynamically measured level of available bandwidth for access to the memory system.

14. (Original) A method of processing a set of data-items, in which each data-item is associated with a respective data address in a range of data addresses, the method comprising

- providing a memory system that has memory addresses comprising a subset of equidistant preferred starting addresses from which multi-address memory transfers can be started exclusively, or with less overhead than from other addresses than the preferred starting addresses;
- storing compressed blocks in the memory system, addresses used for each respective one of the blocks starting from a respective one of the preferred starting addresses, each block representing compressed data-items associated with data addresses in a respective sub-range of the range, the sub-ranges being successively contiguous, each particular sub-range having a length corresponding to an address distance between the preferred starting address from which the particular block that represents the data-items in the particular sub-range starts and the preferred starting address from which a next one the blocks for a next successive sub-range starts, leaving memory addresses not occupied by the particular block in between.

15. (Original) A method according to Claim 14, comprising

- processing decompressed data-items derived from the blocks;
- retrieving a required one of the blocks from the memory system for said processing, by means of a multi-address memory transfer starting from the preferred starting address starting from which the required one of the blocks is stored;
- terminating the multi-address memory transfer for the required one of the blocks according to a length of the required one of the blocks, leaving content of memory addresses directly

following addresses used for the required one of the blocks untransferred.

16. (Original) A method according to Claim 14, comprising storing information representing a length of the required one of the blocks with the required one of the blocks in the memory system for transfer in the multi-address memory transfer.

17. (Original) A method according to Claim 14, comprising storing information representing the length of the required one of the blocks with a logically preceding one of the blocks from which data-items are normally processed during said processing preceding data-items from the required one of the blocks, for transfer in a multi-address memory transfer for the logically preceding one of the blocks.

18. (Original) A method according to Claim 17, comprising

reading the information from the logically preceding one of the blocks;

- sending a transfer length selection signal selected dependent on the information to the memory system at the start of the multi address memory transfer for the required one of the blocks.

19. (Original) A method according to Claim 14, wherein lossy block compression of uncompressed data is used to generate the blocks.

20. (Original) A method according to Claim 14, wherein variable length block compression of uncompressed data is used to generate the blocks.

21. (Original) A method according to Claim 20, wherein a compression ratio of the variable length block compression is dynamically adjusted according to dynamically available bandwidth for access to the memory system.

22. (Currently amended) A computer program product comprising machine instructions for controlling memory transfers and decompression according to the method of ~~any one of Claims 14 to 21~~ claim 14.